Winbond
ExpressCard™
Power Interface Switch
W83L351 Series

Winbond Electronics Corp.

W83L351 Series

Data Sheet Revision History

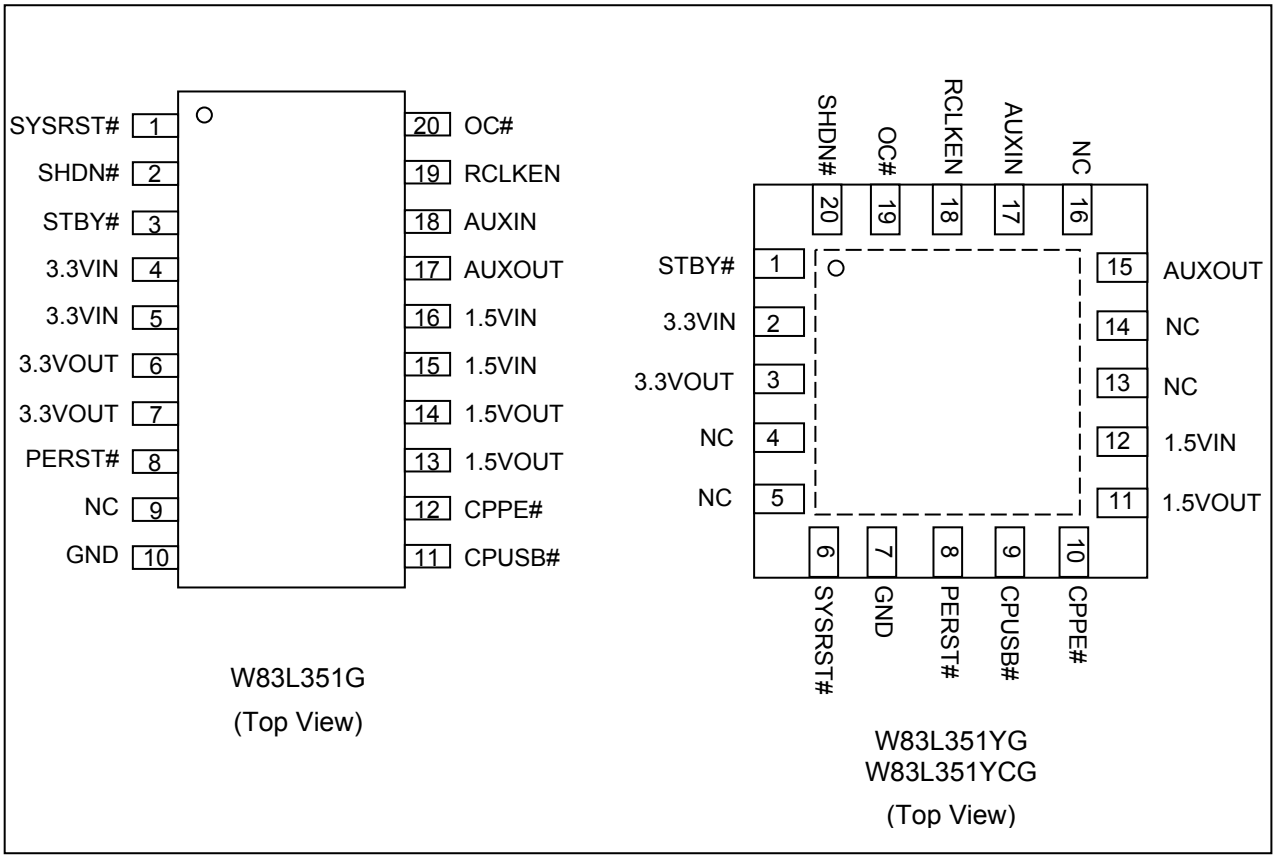
NO	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1.	All	Apr. /07	1.0	N.A	All versions before 1.0 are preliminary versions.
2	28	July 5, 2007	1.1		Update the ordering information and add the taping spec.
3					
4					
5					
6					
7					

Table of Contents-

1. FEATURES

- Meets the ExpressCard™ Standard (ExpressCard|34 or ExpressCard|54)
- Compliant with the ExpressCard™ Compliance Checklists
- ExpressCard Compliance ID: EC100098 (W83L351G), EC100115 (W83L351YG/YCG)
- Fully Satisfies the ExpressCard™ Implementation Guidelines
- Supports System with WAKE Function
- TTL-Logic Compatible Inputs
- Short Circuit and Thermal Protection
- 0℃ to 70℃ Ambient Operating Temperature Range
- Available in a 20-pin TSSOP or a 20-pin QFN

2. PIN CONFIGURATION AND DESCRIPTION



SYMBOL	PIN		I/O	FUNCTION
	G	YG YCG		
SYSRST#	1	6	I(*)	System Reset input – active low, logic level signal. Internally pulled up to AUXIN. This input is driven by the host system and directly affects PERST#. Asserting SYSRST# (logic low) forces PERST# to assert. RCLKEN is not affected by the assertion of SYSRST#.
SHDN#	2	20	I(*)	Shutdown input – active low, logic level signal. Internally pulled up to AUXIN. When asserted (logic low), this input instructs the power switch to turn off all voltage outputs and the discharge FETs are activated.

Continued

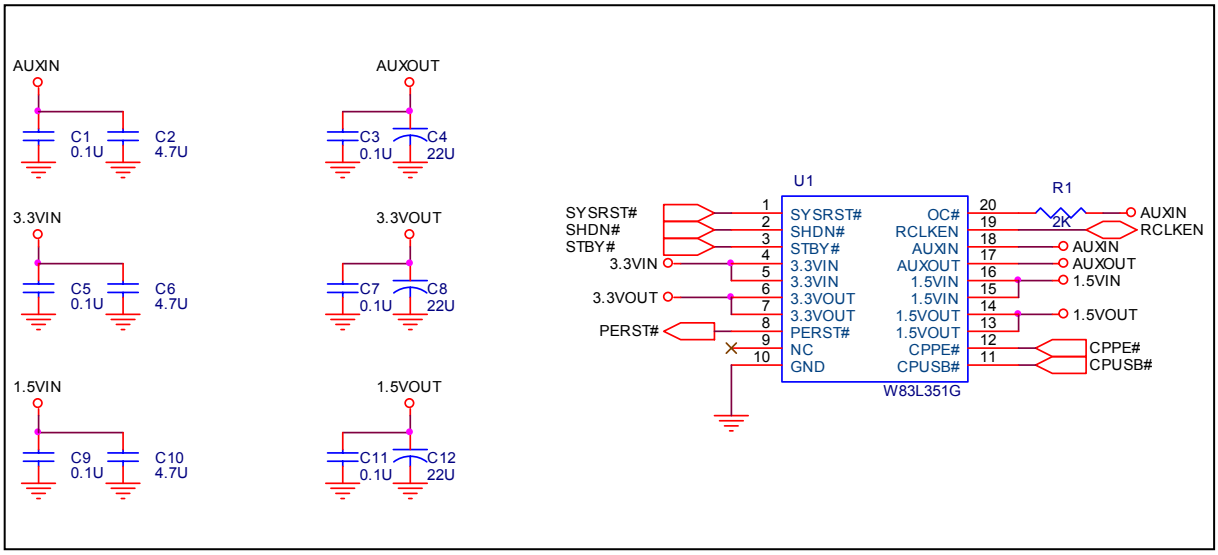
SYMBOL	PIN		I/O	FUNCTION
	G	YG YCG		
STBY#	3	1	I(*)	Standby input – active low, logic level signal. Internally pulled up to AUXIN. When asserted (logic low) after the card is inserted, this input places the power switch in standby mode by turning off the 3.3V and 1.5V power switches and keeping the AUX switch on. If the signal is asserted prior to the card being present, STBY# places the power switch in OFF Mode by turning off the AUX, 3.3V, and 1.5V power switches.
PERST#	8	8	O	A logic level power good (with delay). When powered up, this output remains asserted (logic level low) until all power rails are within the tolerance. Once all power rails are within the tolerance and RCLKEN has been released (logic high), PERST# is de-asserted (logic high) after a time delay, as shown in the parametric table. When powered down, this output is asserted whenever any of the power rails drops below their voltage tolerance. The PERST# signal is an output from the host system and an input to the ExpressCard module. This signal is only used by PCI Express-based modules and its function is to place the ExpressCard module in a reset state. During power up, power down, or whenever power to the ExpressCard module is not stable or not within voltage tolerance limits, the ExpressCard standard requires that PERST# be asserted. As a result, this signal also serves as a power-good indicator to the ExpressCard module, and the relationship between the power rails and PERST# are explicitly defined in the ExpressCard standard. The host can also place the ExpressCard module in a reset state by asserting a system reset SYSRST#. This system reset generates a PERST# signal to the ExpressCard module without disrupting the voltage rails. This is normally called a warm reset. However, in a cold start situation, the system reset can also be used to prolong the assertion time of PERST#.
CPUSB#	11	9	I(*)	Card Present input for USB cards. Internally pulled up to AUXIN. A logic low level on this input indicates that the card present supports the USB functions. When a card is inserted, CPUSB# is physically connected to ground if the card supports USB functions.
CPPE#	12	10	I(*)	Card Present input for PCI Express cards. Internally pulled up to AUXIN. A logic low level on this input indicates that the card present supports the PCI Express functions. When a card is inserted, CPPE# is physically connected to ground if the card supports PCI Express functions.

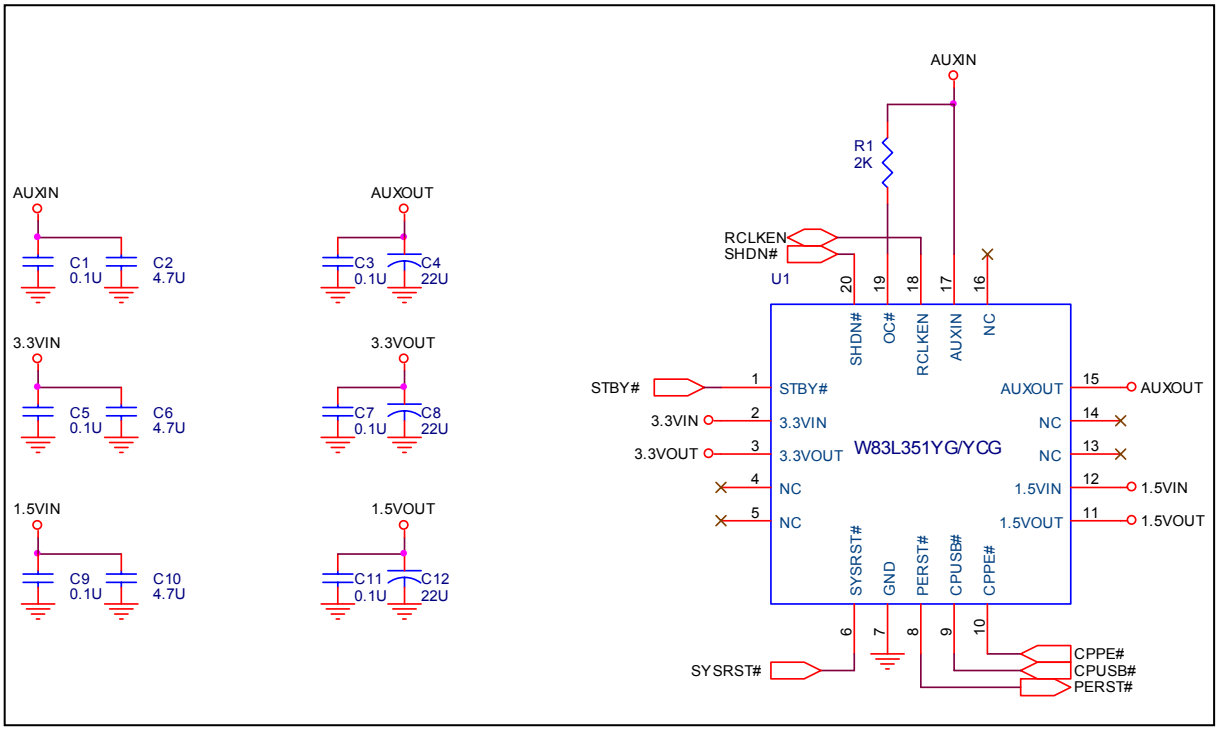
Continued

SYMBOL	PIN		I/O	FUNCTION
	G	YG YCG		
RCLKEN	19	18	I(*)/O	Reference Clock Enable signal. As an output, it is a logic level power good to the host (no delay – open drain). As an input, if the signal is kept inactive (low) by the host, PERST# will be prevented from being de-asserted. Internally pulled up to AUXIN. This pin serves both as an input and an output. When powered up, a discharge FET keeps this signal at a low state as long as any of the output power rails is out of their tolerance range. Once all output power rails are within the tolerance, the switch releases RCLKEN, allowing it to transit to a high state (internally pulled up to AUXIN). The transition of RCLKEN from a low to a high state starts an internal timer for the purpose of de-asserting PERST#. As an input, RCLKEN can be kept low to delay the start of the PERST# internal timer. Because RCLKEN is internally connected to a discharge FET, this pin can only be driven low and should never be driven high as a logic input. When an external circuit drives this pin low, RCLKEN becomes an input; otherwise, this pin is an output.
OC#	20	19	OD	Over current status output (open drain). This pin is an open-drain output. When any of the three power switches (AUX, 3.3V, and 1.5V) is in an over current condition, OC# is asserted (logic low) by an internal discharge FET with a deglitch delay. Otherwise, the discharge FET is open, and the pin can be pulled up to a power supply through an external resistor.
3.3VIN	4, 5	2	I	Primary voltage source, 3.3V input for 3.3VOUT
1.5VIN	15,16	12	I	Secondary voltage source, 1.5V input for 1.5VOUT
AUXIN	18	17	I	Auxiliary voltage source, AUX input for AUXOUT and chip power.
3.3VOUT	6, 7	3	O	Switched output that delivers 0V, 3.3V or high impedance to the card.
1.5VOUT	13, 14	11	O	Switched output that delivers 0V, 1.5V or high impedance to the card.
AUXOUT	17	15	O	Switched output that delivers 0V, AUX or high impedance to the card.
GND	10	7		Ground
NC	9	4, 5, 13, 14, 16		No connection

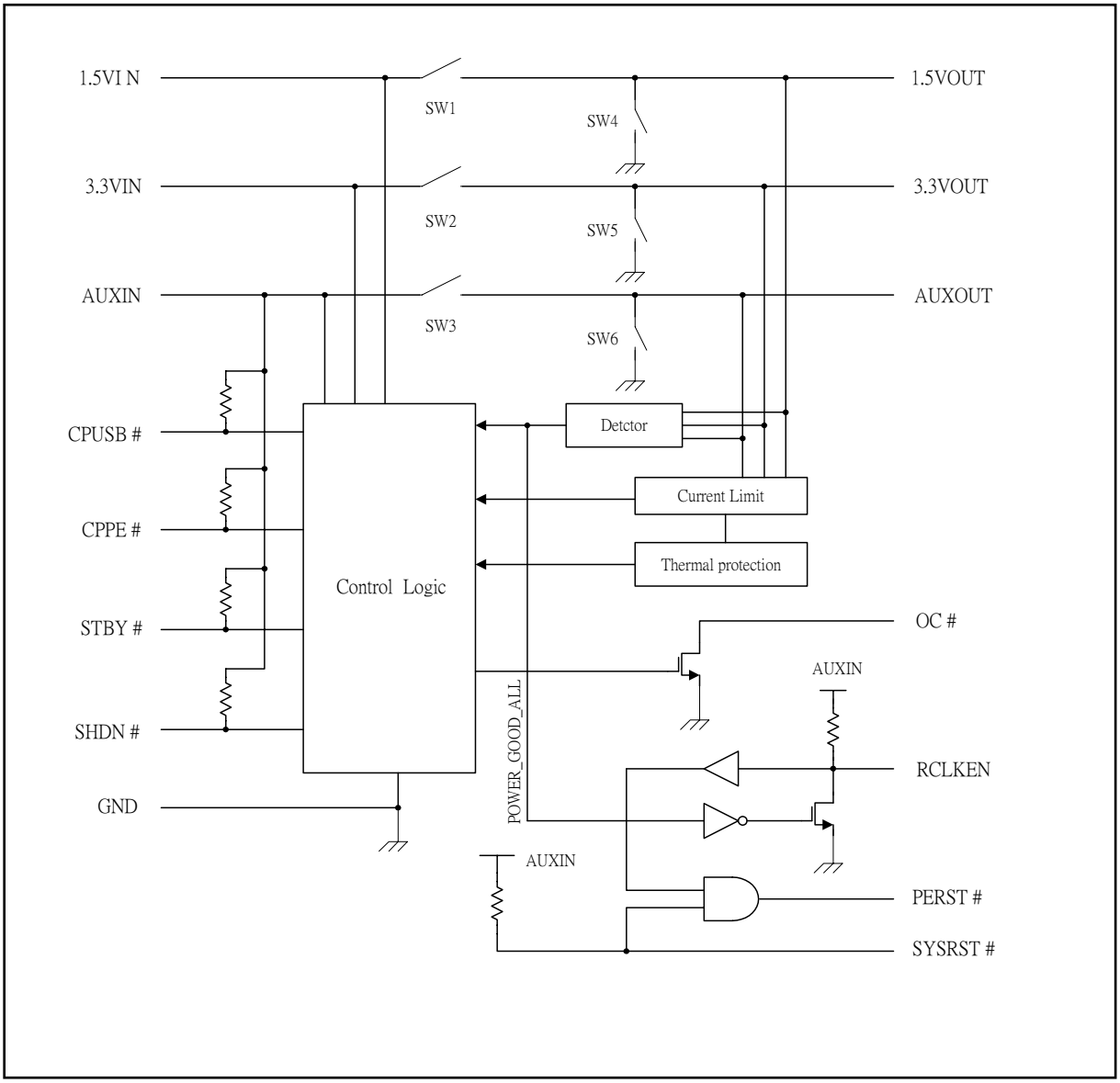
Notice: (*) Be aware that no input pins can be driven HIGH before the Auxiliary voltage is VALID.

3. APPLICATION CIRCUIT





4. INTERNAL BLOCK DIAGRAM



5. ABSOLUTE MAXIMUM RATINGS

ITEM	SYMBOL	RATING	UNIT
Input Voltage	$V_{I(3.3VIN)}$	-0.3 to 6	V
	$V_{I(1.5VIN)}$	-0.3 to 6	V
	$V_{I(AUXIN)}$	-0.3 to 6	V
Logic Input/Output Voltage		-0.3 to 6	V
Output Voltage	$V_{O(3.3VOUT)}$	-0.3 to 6	V
	$V_{O(1.5VOUT)}$	-0.3 to 6	V
	$V_{O(AUXOUT)}$	-0.3 to 6	V
Output Current	$I_{O(3.3OUT)}$	Internally limited	
	$I_{O(1.5OUT)}$	Internally limited	
	$I_{O(AUXOUT)}$	Internally limited	
Operating Temperature Range	T_{opt}	0 to 70	℃
Electrostatic discharge protection	Human Body Mode	±2	kV
	Machine Mode	±200	V
	Latch-Up	±100	mA

6. RECOMMENDED OPERATING CONDITIONS

ITEM			MIN	MAX	UNIT
Input Voltage	$V_{I(3.3VIN)}$	3.3VIN is only required for its respective functions	3	3.6	V
	$V_{I(1.5VIN)}$	1.5VIN is only required for its respective functions	1.35	1.65	
	$V_{I(AUXIN)}$	AUXIN is required for all circuit operations	3	3.6	
Continuous output current	$I_{O(3.3VOUT)}$	TJ=120℃	0	1.3	A
	$I_{O(1.5VOUT)}$		0	650	mA
	$I_{O(AUXOUT)}$		0	275	mA

7. ELECTRICAL CHARACTERISTICS

T_A = 25°C, $V_{I\ (3.3VIN)}$ = $V_{I\ (AUXIN)}$ = 3.3 V, $V_{I\ (1.5VIN)}$ = 1.5 V, $V_{I\ (SHDN\#)}$, $V_{I\ (STBY\#)}$ = 3.3 V, $V_{I\ (CPPE\#)}$ = $V_{I\ (CPUSB\#)}$ = 0 V, $V_{I\ (SYSRST)}$ = 3.3 V, OC# and RCLKEN and PERST# are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power switch resistance	3.3VIN to 3.3VOUT with two switches on for dual		TA = 25°C, I = 1305 mA each		90		mΩ
			TA = 70°C, I = 1305 mA each			105	
	1.5VIN to 1.5VOUT with two switches on for dual		TA = 25°C, I = 660 mA each		90		
			TA = 70°C, I = 660 mA each			110	
	AUXIN to AUXOUT with two switches on for dual		TA = 25°C, I = 285 mA each		110		
			TA = 70°C, I = 285 mA each			126	
I_{OS} Short – circuit output current	$I_{OS(3.3VOUT)}$ (steady-state value)		Output powered into a short	1.35	1.7	2.5	A
	$I_{OS(1.5VOUT)}$ (steady-state value)			0.67	1.1	1.3	A
	$I_{OS(AUXOUT)}$ (steady-state value)			275	400	600	mA
Thermal Shutdown	Trip point, T_J		Rising temperature, not in over current condition		155		°C
			Over current condition		130		
	Hysteresis				10		
I_I Total input quiescent current (Note: 1)	Normal operation	$I_{I(AUXIN)}$	Outputs are unloaded (include CPPE# and CPUSB# logic pull-up currents)		140	210	uA
		$I_{I(3.3VIN)}$			10.5	15	
		$I_{I(1.5VIN)}$			2.2	10	
	Shutdown mode	$I_{I(AUXIN)}$	CPUSB# = CPPE# = 0 V SHDN# = 0 V (discharge FETs are on) (include CPPE# and CPUSB# logic pull-up currents and SHDN# pull-up current)		170	270	uA
		$I_{I(3.3VIN)}$			6	10	
		$I_{I(1.5VIN)}$			2.2	10	
	Standby mode (1)	$I_{I(AUXIN)}$	CPUSB# = CPPE# = 0 V STBY# = 0 V (include CPPE# and CPUSB# logic pull-up currents and STBY# pull-up current)		170	270	uA
		$I_{I(3.3VIN)}$			6	10	
		$I_{I(1.5VIN)}$			2.2	10	
	Standby mode (2)	$I_{I(AUXIN)}$	CPUSB# = CPPE# = 0 V 3.3VIN = 0 V (include CPPE# and CPUSB# logic pull-up currents)		160	210	uA
		$I_{I(3.3VIN)}$			0	0.1	
		$I_{I(1.5VIN)}$			2.2	10	

Continued

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Standby mode (3)	$I_{I(AUXIN)}$	CPUSB# = CPPE# = 0 V 1.5VIN = 0 V (include CPPE# and CPUSB# logic pull-up currents)		160	210	uA
		$I_{I(3.3VIN)}$			6	10	
		$I_{I(1.5VIN)}$			0	0.1	
$I_{lkg(FWD)}$ Forward leakage current	$I_{I(AUXIN)}$		SHDN# = 3.3 V, CPUSB# = CPPE# = 3.3 V (no card present, discharge FETs are on);current measured at input pins, includes RCLKEN pull- up current		22	50	uA
	$I_{I(3.3VIN)}$				0	50	
	$I_{I(1.5VIN)}$				0	50	
LOGIC SECTION (SYSRST, SHDN#, STBY#, PERST#, RCLKEN , OC#, CPUSB#, CPPE#)							
Logic input supply current	$I_{(SYSRS\#)}$	Input	SYSRST# = 3.6 V, sinking		0		uA
			SYSRST# = 0 V, sourcing	10	17.5	30	
	$I_{(SHDN\#)}$	Input	SHDN# = 3.6 V, sinking		0		uA
			SHDN# = 0 V, sourcing	10	17.5	30	
	$I_{(STBY\#)}$	Input	STBY# = 3.6 V, sinking		0		uA
			STBY# = 0 V, sourcing	10	17.5	30	
	$I_{(RCLKEN)}$	Input	RCLKEN = 0 V, sourcing	10	18	30	uA
	$I_{(CPUSB\#)}$ or $I_{(CPPE\#)}$	inputs	CPUSB# or CPPE# = 0 V, sinking		0		uA
			CPUSB# or CPPE# = 3.6 V, sourcing	10	17.5	30	
Logic input voltage	High level			2			V
	Low level					0.8	
RCLKEN output low voltage		Output	IO(RCLKEN) = 60 µA			0.4	V
PERST# assertion threshold of output voltage (PERST# asserted when any output voltage falls below the threshold)			3.3VOUT falling	2.7		3	V
			AUXOUT falling	2.7		3	
			1.5VOUT falling	1.2		1.5	
PERST# assertion delay from output voltage			3.3VOUT, AUXOUT, 1.5VOUT falling			500	ns
PERST# de-assertion delay from output voltage			3.3VOUT, AUXOUT, or 1.5VOUT rising within tolerance	1	20		ms

Continued

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PERST# assertion delay from SYSRST#	Max time from SYSRST asserted		25	500	ns
$t_{W(PERST\#)}$ PERST# minimum pulse width	3.3VOUT, AUXOUT, or 1.5VOUT falling out of tolerance or triggered by SYSRST#	100	340		us
PERST# output low voltage	$I_{O(PERST\#)}$ = 500 µA			0.4	V
PERST# output high voltage		2.4			V
OC# output low voltage	$I_{O(OC\#)}$ = 2 mA			0.4	V
OC# deglitch	Falling into or out of an over current condition		20		ms
UNDERVOLTAGE LOCKOUT (UVLO)					
3.3VIN UVLO	3.3VIN level, below which 3.3VIN and 1.5VIN switches are off	2.6		2.9	V
1.5VIN UVLO	1.5VIN level, below which 3.3VIN and 1.5VIN switches are off	1.0		1.25	
AUXIN UVLO	AUXIN level, below which all switches are off	2.6		2.9	
UVLO hysteresis			100		mV

Note 1: In the Shutdown mode or the Standby mode (1), the AUXIN quiescent current includes a normal operation current, SHDN# or STBY# internal pull-up current and RCLKEN internal pull-up current. In the Standby modes (2) & (3), the AUXIN quiescent current includes a normal operation current and a RCLKEN internal-up current.

8. SWITCHING CHARACTERISTICS

T_A = 25°C, $V_{I\ (3.3VIN)}$ = $V_{I\ (AUXIN)}$ = 3.3 V, $V_{I\ (1.5VIN)}$ = 1.5 V, $V_{I\ (SHDN\#)}$, $V_{I\ (STBY\#)}$ = 3.3 V, $V_{I\ (CPPE\#)}$ = $V_{I\ (CPUSB\#)}$ = 0 V, $V_{I\ (SYSRST)}$ = 3.3 V, OC# and RCLKEN and PERST# are open, all voltage outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r Output rise times	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=0.1uF, $I_{O(3.3VOUT)}$=0A	0.1		6	ms
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=0.1uF, $I_{O(AUXOUT)}$=0A	0.1		6	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=0.1uF, $I_{O(1.5VOUT)}$=0A	0.1		6	
	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=100uF, R_L=$V_{I(3.3VIN)}$/1A	0.1		6	
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=100uF, R_L=$V_{I(AUXININ)}$/0.250A	0.1		6	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=100uF, R_L=$V_{I(1.5VIN)}$/0.500A	0.1		6	
t_f Output fall times when card removed (both CPUSB# and CPPE# de-asserted)	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=0.1uF, $I_{O(3.3VOUT)}$=0A	10		150	us
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=0.1uF, $I_{O(AUXOUT)}$=0A	10		150	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=0.1uF, $I_{O(1.5VOUT)}$=0A	10		150	
	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=20uF, $I_{O(3.3VOUT)}$=0A	5		30	ms
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=20uF, $I_{O(AUXOUT)}$=0A	5		30	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=20uF, $I_{O(1.5VOUT)}$=0A	5		30	
t_f Output fall times when SHDN# asserted (card is present)	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=0.1uF, $I_{O(3.3VOUT)}$=0A	10		150	us
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=0.1uF, $I_{O(AUXOUT)}$=0A	10		150	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=0.1uF, $I_{O(1.5VOUT)}$=0A	10		150	
	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=100uF, R_L=$V_{I(3.3VIN)}$/1A	0.1		3	ms
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=100uF, R_L=$V_{I(AUXININ)}$/0.250A	0.1		3	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=100uF, R_L=$_{VI(1.5VIN)}$/0.500A	0.1		3	
$T_{pd(on)}$ Turn on propagation delay	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=0.1uF, $I_{O(3.3VOUT)}$=0A	0.1		6	ms
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=0.1uF, $I_{O(AUXOUT)}$=0A	0.1		6	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=0.1uF, $I_{O(1.5VOUT)}$=0A	0.1		6	
	3.3VIN to 3.3VOUT	$C_{L(3.3VOUT)}$=100uF, R_L=$V_{I(3.3VIN)}$/1A	0.1		6	
	AUXIN to AUXOUT	$C_{L(AUXVOUT)}$=100uF, R_L=$V_{I(AUXININ)}$/0.250A	0.1		6	
	1.5VIN to 1.5VOUT	$C_{L(1.5VOUT)}$=100uF, R_L=$_{VI(1.5VIN)}$/0.500A	0.1		6	

9. FUNCTIONAL TRUTH TABLES

Truth Table for Voltage Outputs

VOLTAGES INPUTS (1)			LOGIC INPUTS			VOLTAGE OUTPUTS(2)			MODE(3)
AUXIN	3.3VIN	1.5VIN	SHDN#	STBY#	CP# (4)	AUXOUT	3.3VOUT	1.5VOUT	
Off	X	X	X	X	X	Off	Off	Off	Off
On	Off	Off	1	1	X	Off	Off	Off	Off
On	On	On	1	0	0	Off	Off	Off	Off(5)
On	On	On	1	0	X	Off	Off	Off	Off(6)
On	X	X	0	X	X	GND	GND	GND	Shutdown
On	X	X	1	X	1	GND	GND	GND	No Card
On	On	On	1	0	0	On	Off	Off	Standby
On	On → Off	On → Off	1	1	0	On	Off	Off	Standby(7)
On	On	On	1	1	0	On	On	On	Card Inserted

(1) For input voltages, *On* means the respective input voltage is higher than its turn on threshold voltage; otherwise, the voltage is *Off* (for AUX input, *Off* means the voltage is close to zero volt).

(2) For output voltages, *On* means the respective power switch is turned on so the input voltage is connected to the output; *Off* means the power switch and its output discharge FET are both off; *Gnd* means the power switch is off but the output discharge FET is on so the voltage on the output is pulled down to 0 V.

(3) *Mode* assigns each set of input conditions and respective output voltage results to a different name. These modes are referred to as input conditions in the following *Truth Table for Logic Outputs*.

(4) CP# = CPUSB# and CPPE# equal to 1 when both CPUSB# and CPPE# signals are logic high, or equal to 0 when either CPUSB# or CPPE# is low.

(5) STBY# is asserted (logic low) prior to the card being present.

(6) STBY# is asserted (logic low) prior to the voltage inputs being present.

(7) The card is inserted prior to the removal of the Primary or Secondary power (either 3.3VIN or 1.5VIN or both) at the input of the ExpressCard power switch, then only the primary and secondary power (both 3.3VOUT and 1.5VOUT) are removed and the auxiliary power is sent to the ExpressCard slot.

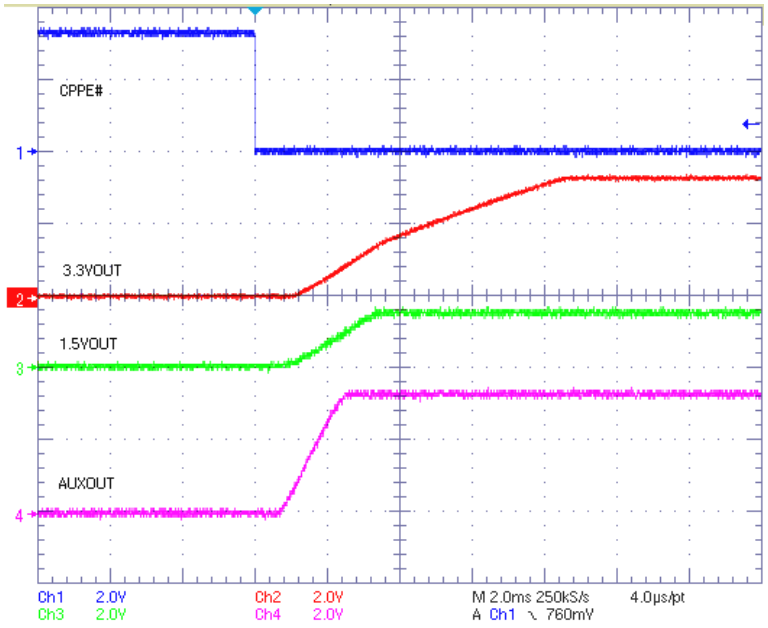
Truth Table for Logic Outputs

INPUT CONDITIONS			LOGIC OUTPUTS	
MODE	**SYSRST#**	**RCLKEN (1)**	**PERST#**	**RCLKEN (2)**
Off	X	X	0	0
Shutdown				
No Card				
Standby				
Card Inserted	0	Hi - Z	0	1
	0	0	0	0
	1	Hi - Z	1	1
	1	0	0	0

(1) RCLKEN as a logic input in this column. RCLKEN is an I/O pin and it can be driven low externally, left open, or connected to high-impedance terminals, such as the gate of a MOSFET. It must not be driven high externally.

(2) RCLKEN as a logic output in this column.

10. TYPICAL OPERATING WAVEFORMS



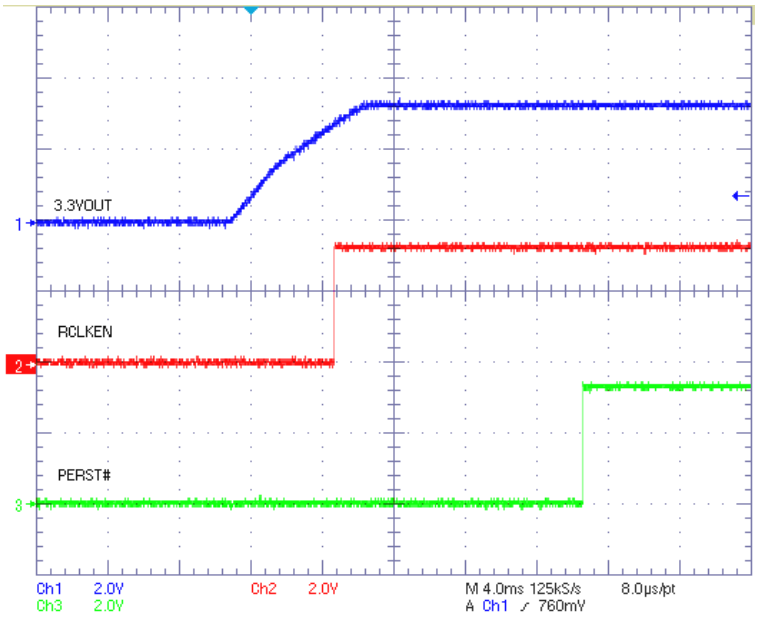
CH1 CPPE#

CH2 3.3VOUT

CH3 1.5VOUT

CH4 AUXOUT

Fig.1 Output Voltage When Card Is Inserted

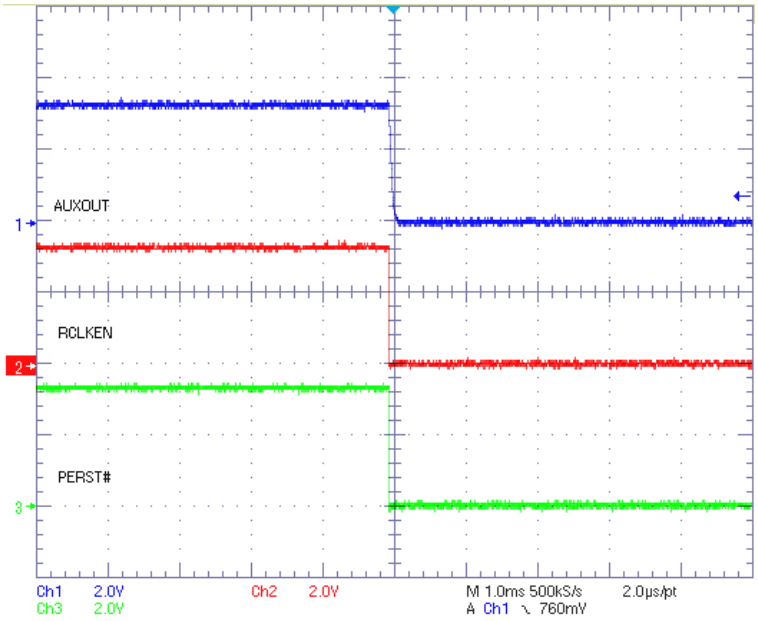


CH1 3.3VOUT

CH2 RCLKEN

CH3 PERST#

Fig.2 RCLKEN and PERST# Voltage During Power Up

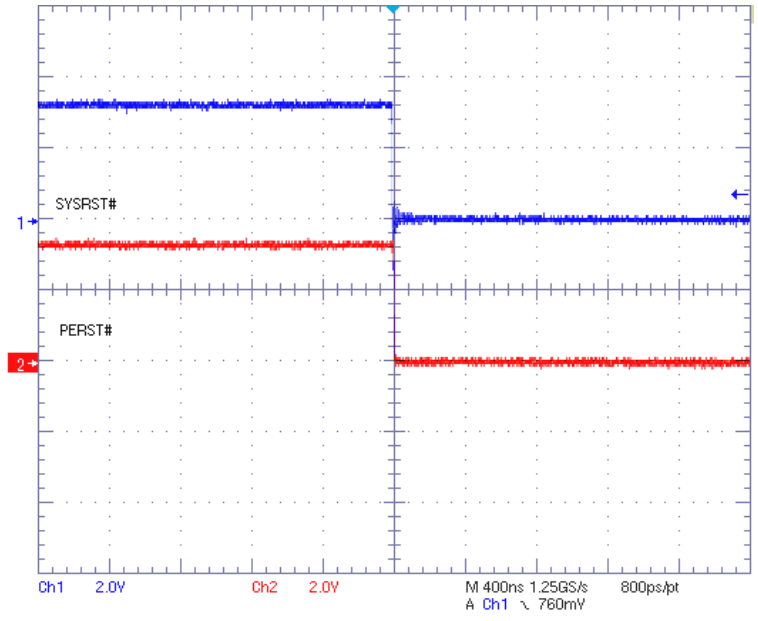


CH1 AUXOUT

CH2 RCLKEN

CH3 PERST#

Fig.3 RCLKEN and PERST# Voltage During Power Down



CH1 SYSRST#

CH2 PERST#

Fig.4 PERST# Asserted by SYSRST# When Power Is On

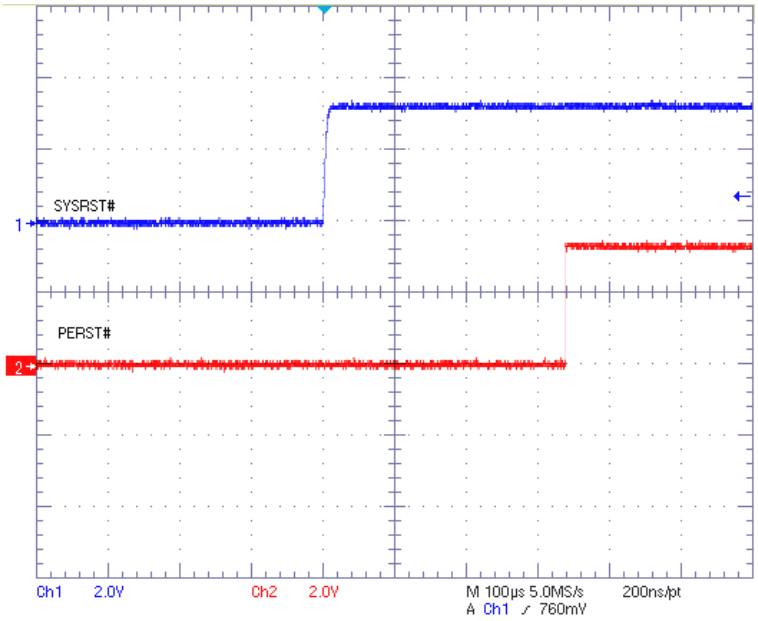


Fig.5 PERST# De-Asserted by SYSRST# When Power Is On

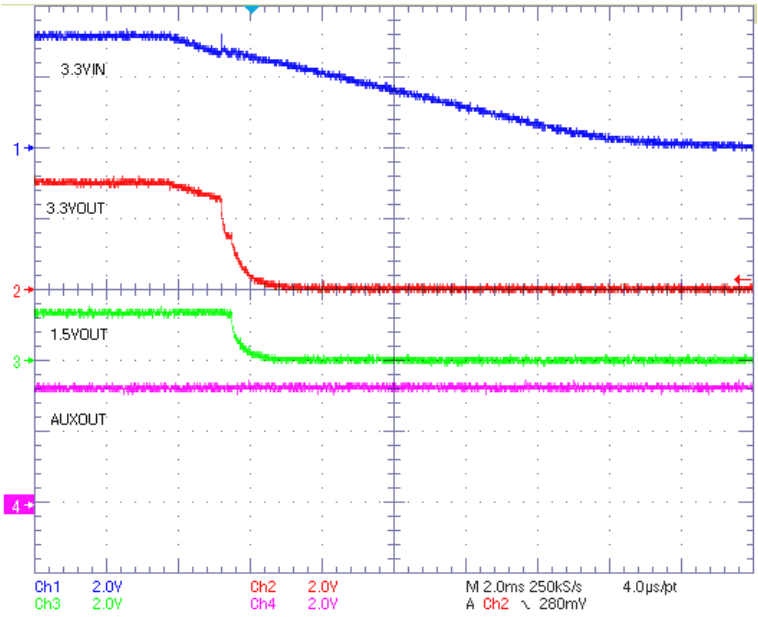
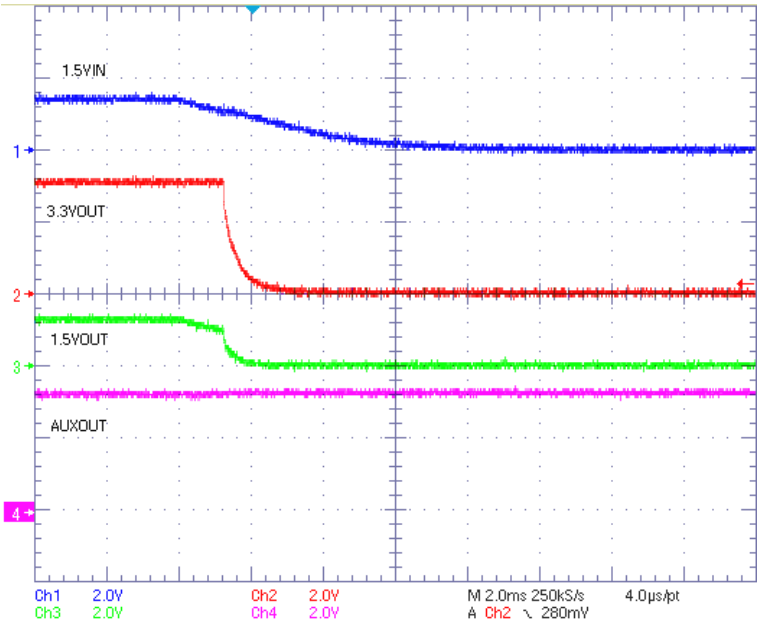


Fig.6 Output Voltage When 3.3VIN Is Removed



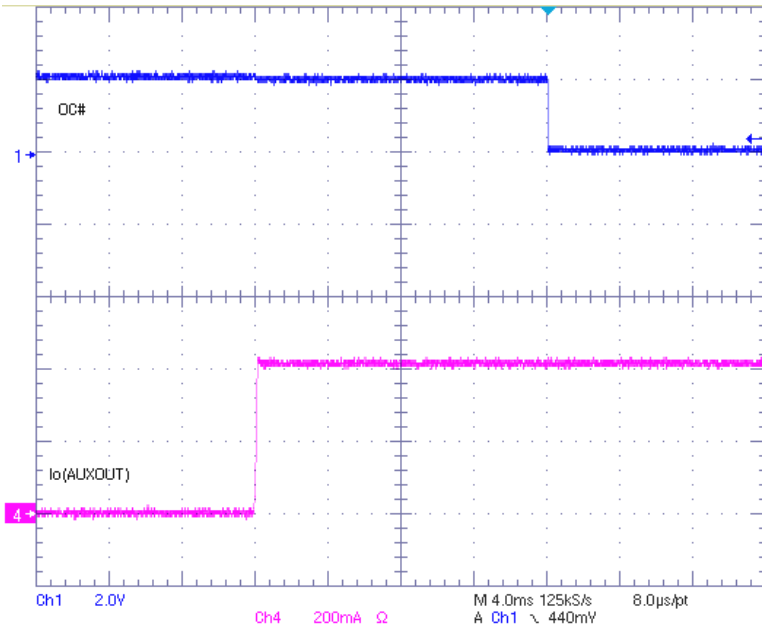
CH1 1.5VIN

CH2 3.3VOUT

CH3 1.5VOUT

CH4 AUXOUT

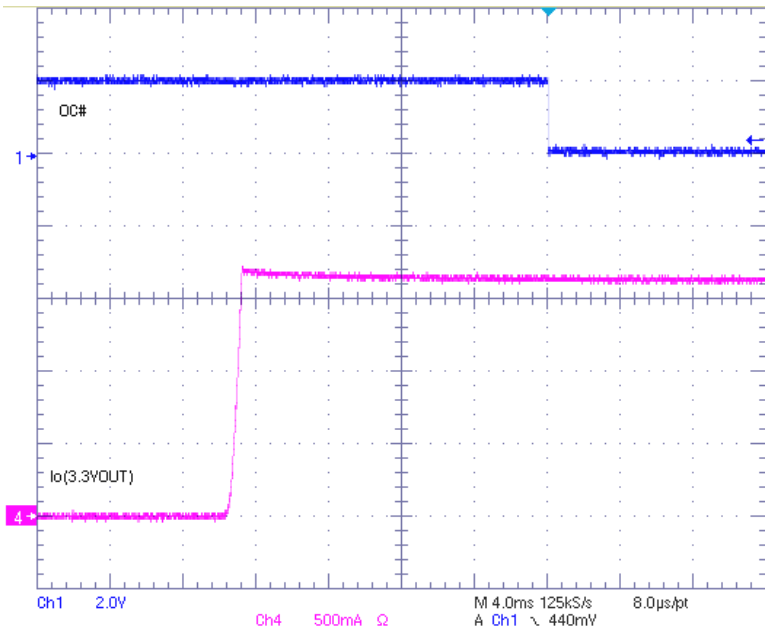
Fig.7 Output Voltage When 1.5VIN Is Removed



CH1 OC#

CH2 AUXOUT

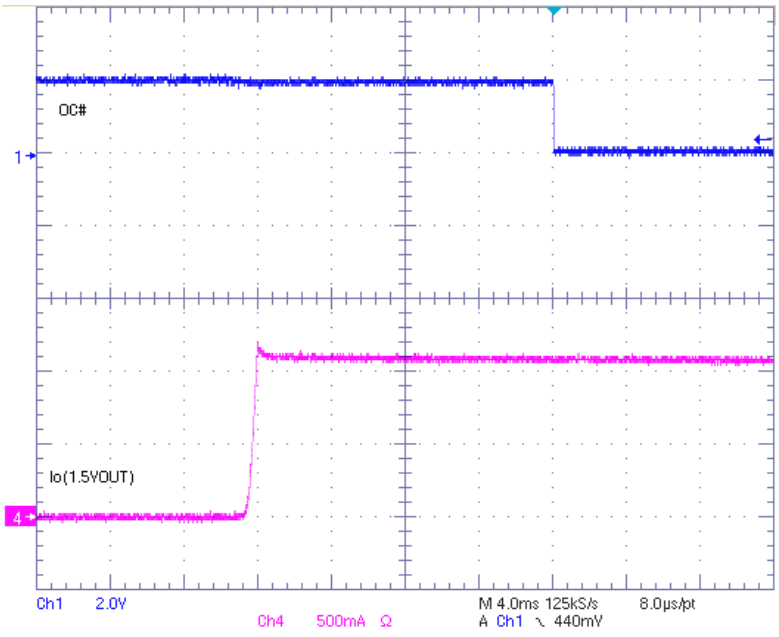
Fig.8 OC# Response When AUXOUT Power Into A Short



CH1 OC#

CH2 3.3VOUT

Fig.9 OC# Response When 3.3VOUT Power Into A Short

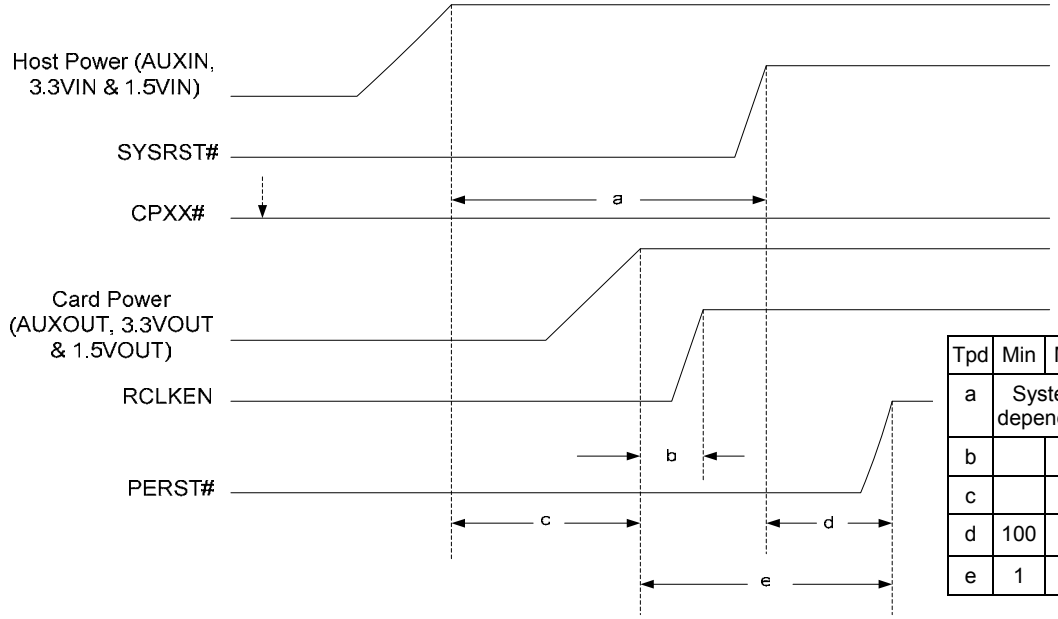


CH1 OC#

CH2 1.5VOUT

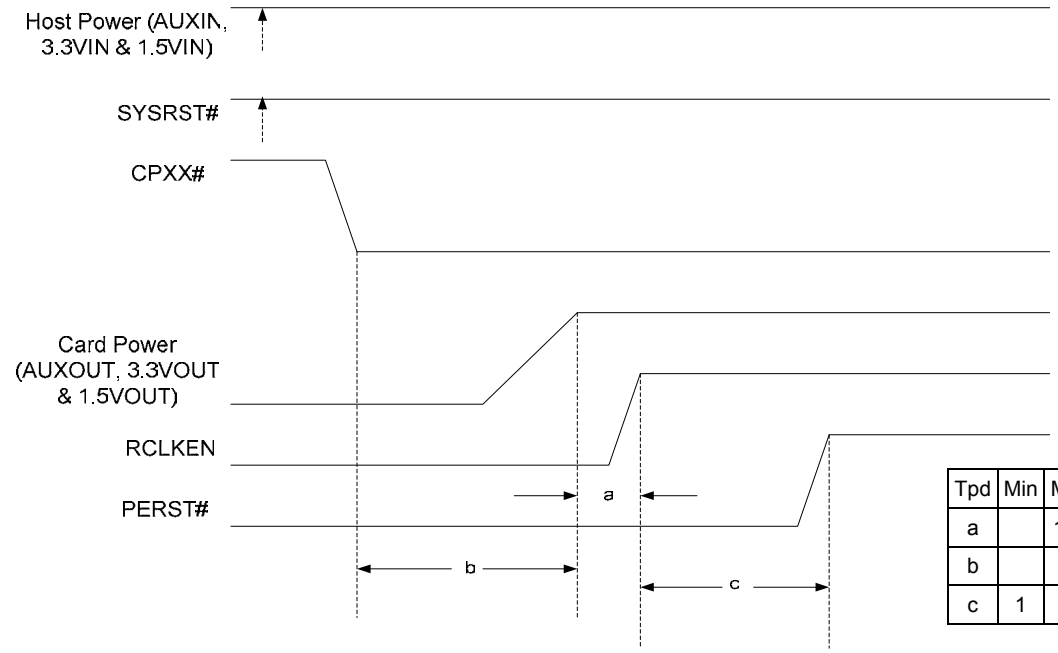
Fig.10 OC# Response When 1.5VOUT Power Into A Short

11. EXPRESSCARD TIMING DIAGRAMS



Tpd	Min	Max	Units
a	System dependent		
b		100	us
c		10	ms
d	100		us
e	1	20	ms

Fig.11 Card Present Before Host Power (Note.1)



Tpd	Min	Max	Units
a		100	us
b		10	ms
c	1	20	ms

Fig.12 Host Power Is On Prior To Card Insertion (Note.2)

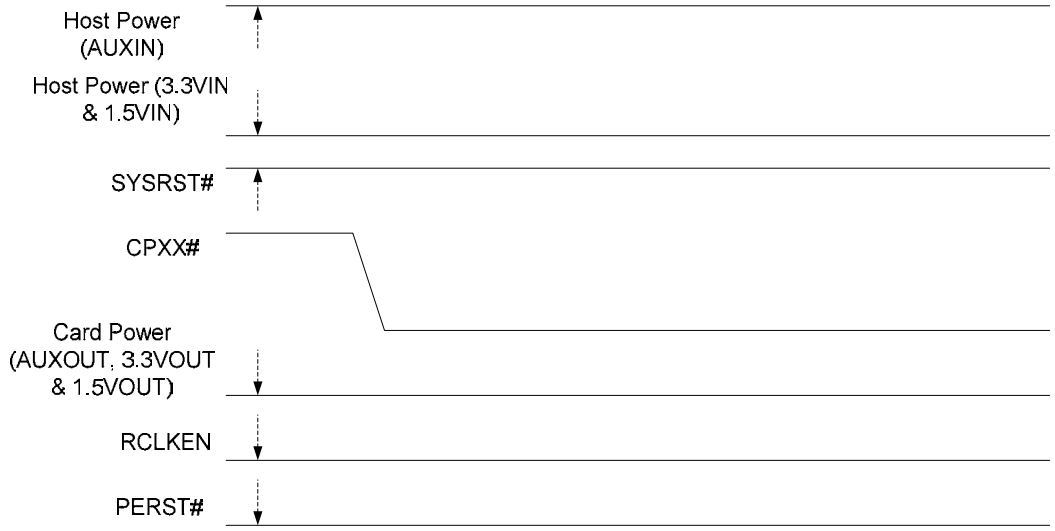
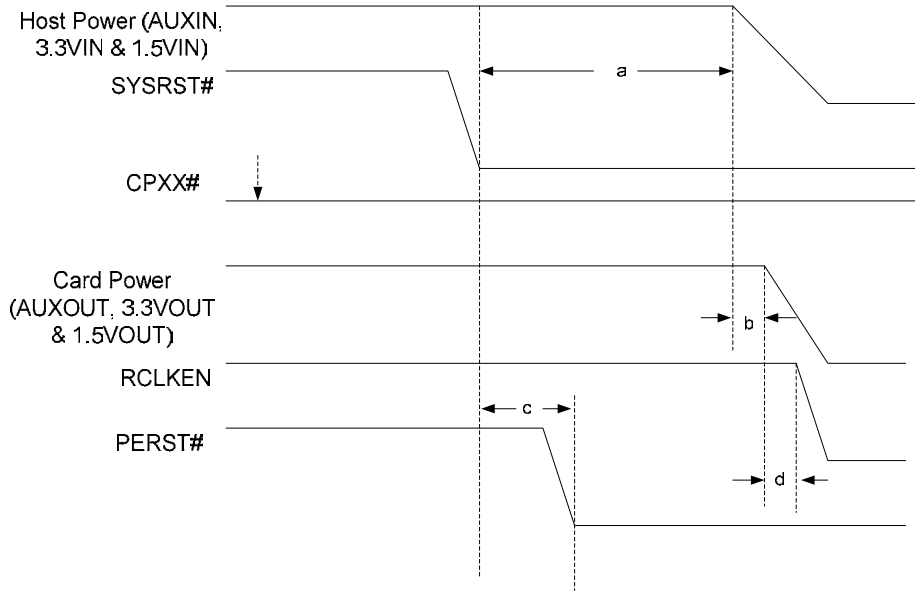
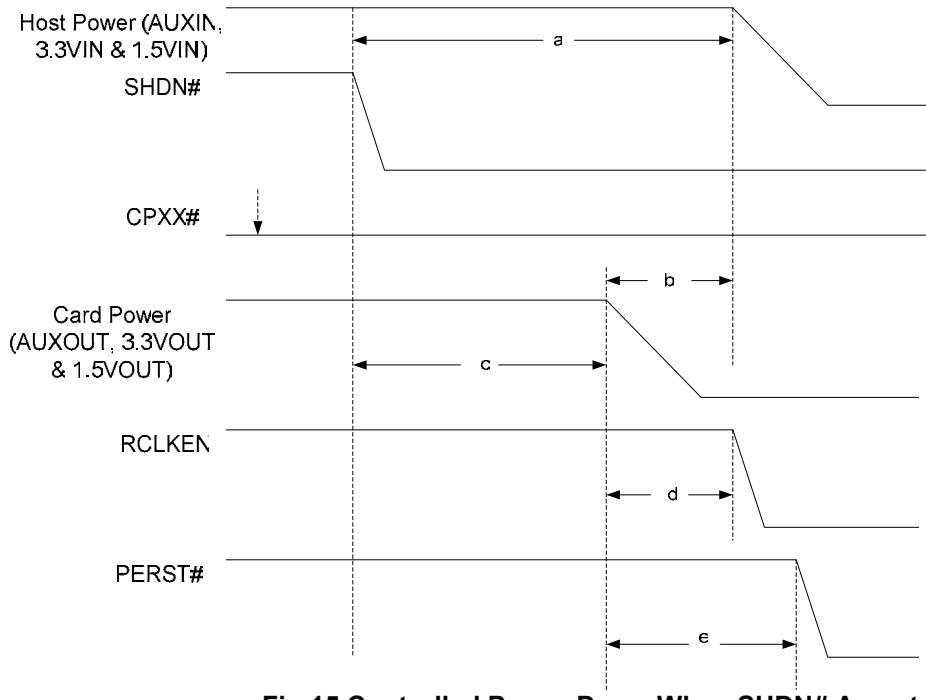


Fig.13 Host System In Standby Prior to Card Insertion



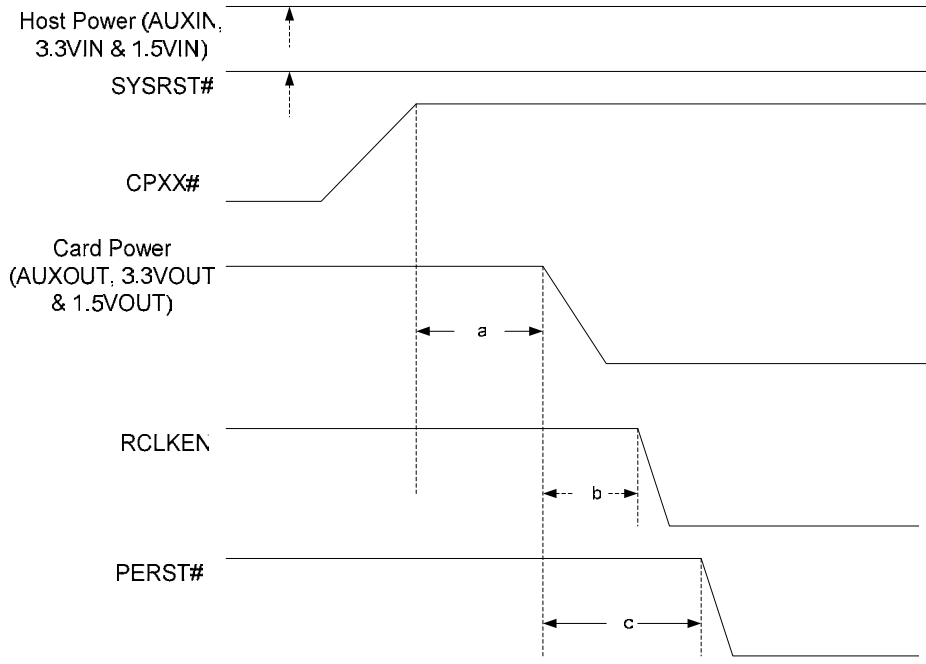
Tpd	Min	Max	Units
a	System dependent		
b	Load dependent		
c		500	ns
d		500	ns

Fig.14 Host Controlled Power Down (Note.3)



Tpd	Min	Max	Units
a	System dependent		
b	System dependent		
c	Load dependent		
d		500	ns
e		500	ns

Fig.15 Controlled Power Down When SHDN# Asserted (Note.4)



Tpd	Min	Max	Units
a	Load dependent		
b		500	ns
c		500	ns

Fig.16 Surprise Card Removal

Note.1: According to the electrical specifications of ExpressCard Standard, the minimum propagation delay time of e (Power stable to PERST# inactive) is 1ms.

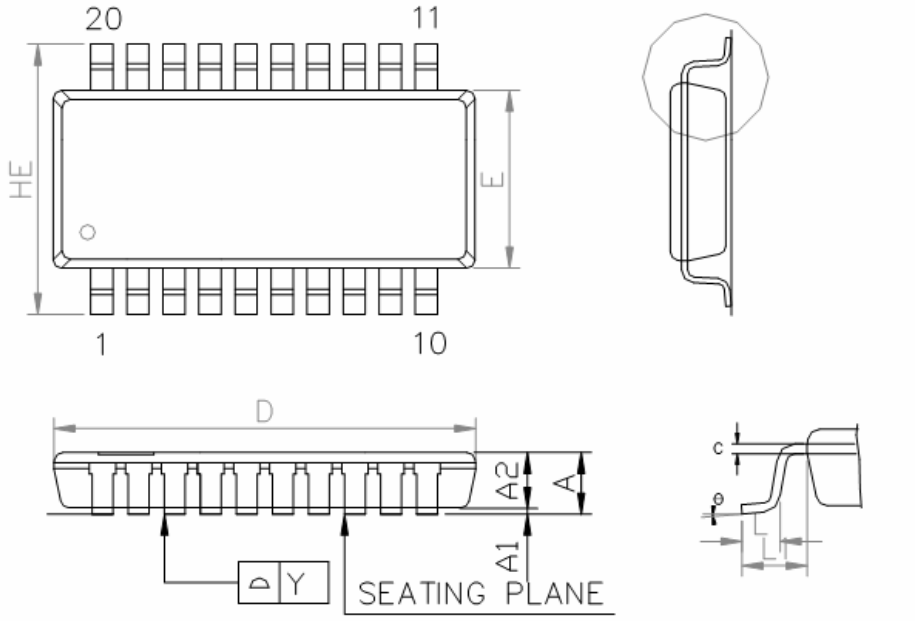
Note.2: RCLKEN could be treated as a power good signal when card power is over 86% of nominal voltage.

Note.3: The propagation delay time of c is SYSRST# assertion to PERST# assertion. The propagation delay time of d is card power is under 86% of nominal voltage to RCLKEN de-assertion.

Note 4: RCLEKN de-assertion is prior to PERST# assertion when card power lost in any situation.

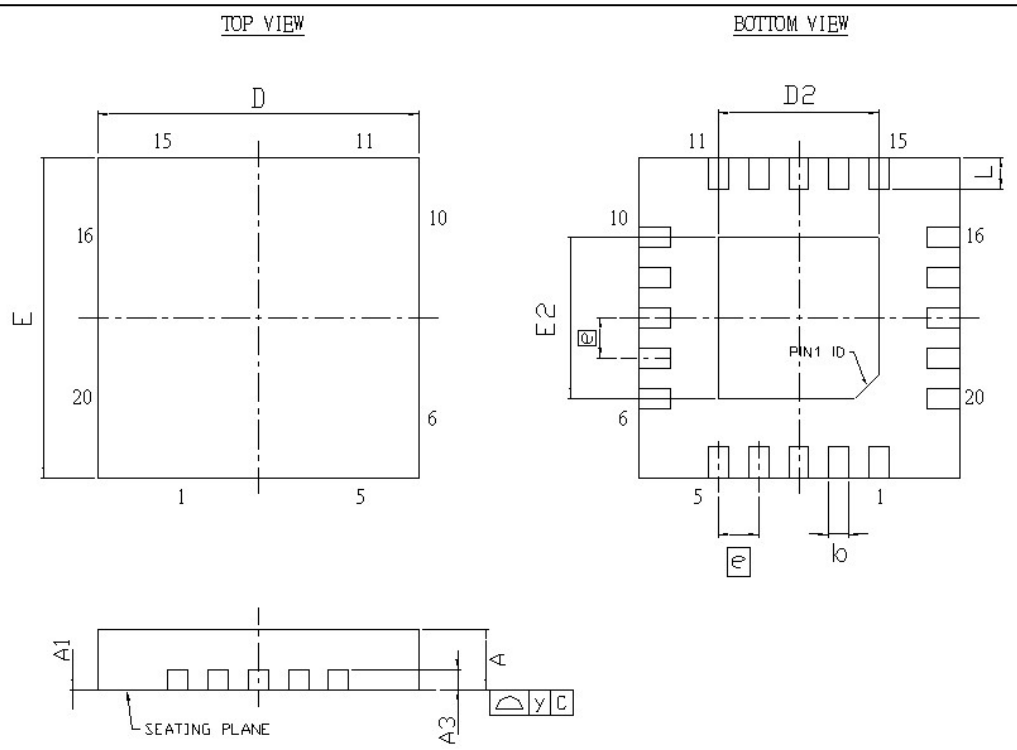
12. PACKAGE DIMENSION

W83L351G - TSSOP20



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1,20	-	-	0.047
A1	0,05	-	0,15	0.002	-	0.006
A2	0.80	0.90	1,05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE		6.40 BSC			0.252 BSC	
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1		1.00 REF			0.039 REF	
b	0.19	-	0.30	0.007	-	0.012
e		0.65 BSC			0.026 BSC	
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y		0.10 BASIC			0.004 BASIC	

W83L351YG - QFN20, Thermal Pad Dimension: 2.0mm X 2.0mm

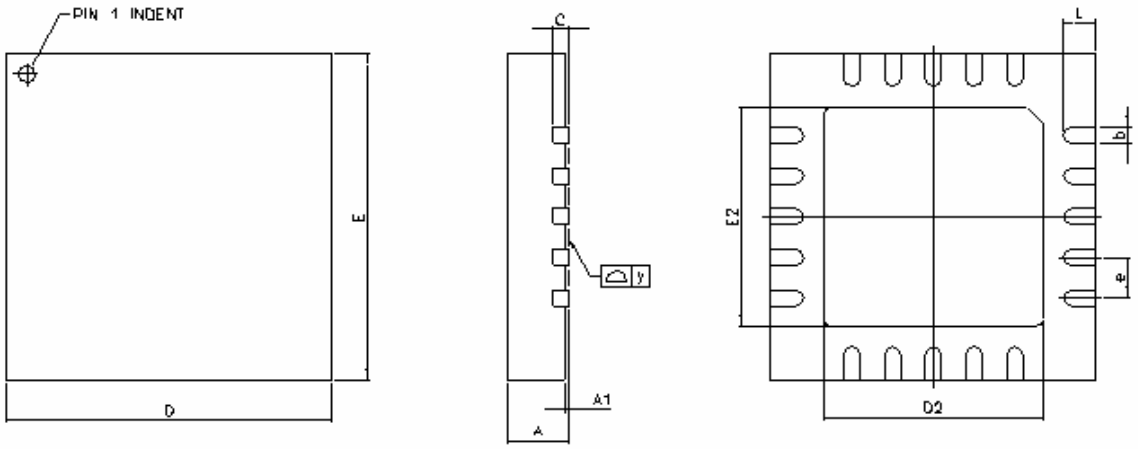


Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

W83L351YCG - QFN20, Thermal Pad Dimension: 2.7mm X 2.7mm

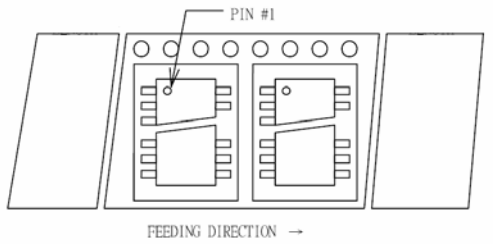


Controlling Dimension :Millimeters

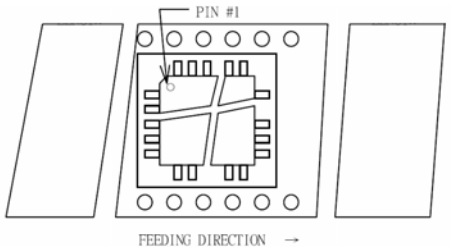
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.02755	0.02952	0.03149
A1	0.00	0.02	0.05	0.00000	0.00078	0.00196
b	0.15	0.23	0.30	0.00590	0.00905	0.01181
C		0.20 REF.			0.00787 REF.	
D	3.90	4.00	4.10	0.15354	0.15748	0.16141
D2	2 65	2.70	2.75	0.10433	0.10629	0.10826
E	3.95	4.00	4.05	0.15551	0.15748	0.15944
E2	2.65	2.70	2.75	0.10433	0.10629	0.10826
e	——	0.50	——	——	0.01968	——
L	0.35	0.40	0.45	0.01377	0.01574	0.01771
y	0.00	——	0.075	0.00000	——	0.00295

Note:D2,E2 by die size difference .

➢ **Taping Specification**



20 Pin TSSOP Package

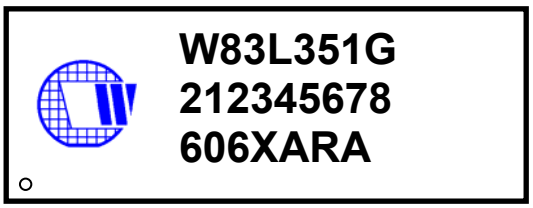


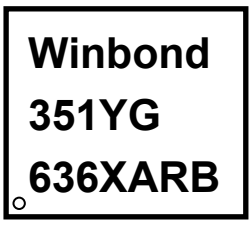
20 Pin QFN Package

13. ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	SUPPLIED AS	PRODUCTION FLOW
W83L351G	20PIN TSSOP (Pb-free package)	E Shape: 74 units/Tube T Shape: 2,500 units/T&R	Commercial, 0℃ to +70 ℃
W83L351YG	20PIN QFN (Pb-free package) Thermal Pad Size: 2.0X2.0 ㎜²	E Shape: 490 units/Tray T Shape: 4,000 units/T&R	Commercial, 0℃ to +70 ℃
W83L351YCG	20PIN QFN (Pb-free package) Thermal Pad Size: 2.7X2.7 ㎜²	E Shape: 490 units/Tray T Shape: 4,000 units/T&R	Commercial, 0℃ to +70 ℃

14. TOP MARKING SPECIFICATION





Left line: Winbond logo

1st line: W83L351G – the part number

2nd line: Chip lot no

3rd line: Tracking code 606 X ARA

606: Packages assembled in Year 06', week 06

X: Assembly house ID

ARA: The IC version

1st line: Winbond – company name

2nd line: 351YG/351YCG – the part number

3rd line: Tracking code 636 X ARB

636: Packages assembled in Year 06', week 36

X: Assembly house ID

ARB: The IC version

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